CLAIMS

What is claimed is:

1.A method of forming an integrated circuit transistor comprising:

depositing a first dielectric layer on a substrate;

etching a gate electrode trench in the first dielectric layer;

depositing a conformal gate dielectric film to line the trench; and

depositing a gate electrode conductor in the trench to cover the gate dielectric film and fill the trench.

2. The method as recited in claim 1 wherein the gate electrode trench etch stops on the underlying substrate.

3. The method as recited in claim 1 wherein the gate electrode trench is extended such that the bottom of the trench forms a depression in the substrate.

4. The method as recited in claim 1 wherein the first dielectric layer comprises one of undoped silicate glass and phospho-silicate glass.

5. The method as recited in claim 1 wherein the gate electrode conductor comprises aluminum.

6. The method as recited in claim 1 wherein the gate electrode conductor comprises one of aluminum, tungsten, and polysilicon.

7. The method as recited in claim 1 further comprising defining a drain and source region in the substrate before depositing the first dielectric layer on the substrate.

8. The method as recited in claim 7 further comprising defining a lightly doped drain region and a punch through implant stop layer in the substrate before depositing the first dielectric layer on the substrate.

9. The method as recited in claim 1 further comprising defining a lightly doped drain region and a punch through implant stop layer in the substrate before depositing the first dielectric layer on the substrate.

10. The method as recited in claim 1 wherein the first dielectric layer is an interlayer dielectric and further comprising forming at least one contact hole in the first interlayer dielectric.

11. The method as recited in claim 10 wherein the at least one contact hole exposes at least one of a source, a drain, or a gate electrode and further comprising forming a salicide on the exposed at least one of a source, a drain, and a gate electrode.

12. The method as recited in claim 1 further comprising etching a channel trench into the substrate beneath the gate electrode trench and epitaxially growing a silicon layer in the channel trench.

13. The method as recited in claim 12 wherein the epitaxially grown silicon layer is a strained silicon layer formed on a SiGe layer grown in the channel trench.

14. The method as recited in claim 12 wherein the epitaxially grown silicon layer is a strained silicon layer formed on a Ge layer grown in the channel trench.

15. The method as recited in claim 14 wherein the strained silicon substrate implant is formed on one of a SiGe or Ge layer.

16. A method of forming a semiconductor integrated circuit, the method comprising:

forming a source and drain diffusion region on a semiconductor substrate;

forming an interlayer dielectric layer on the semiconductor substrate after formation of the source and drain diffusions;

etching a gate electrode trench in the interlayer dielectric layer, the gate electrode trench configured for the placement of a gate electrode to control the current between the source and drain regions;

lining the gate electrode trench with a gate dielectric layer; and

depositing a gate electrode conductive material in the gate electrode trench after lining the trench with the gate dielectric film.

17. The method as recited in claim 16 wherein the gate electrode trench etch stops on the substrate.

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